ABSTRACT

A flash memory device is disclosed that includes a number of columns each of which is connected with a plurality of memory cells. A column selector circuit selects a part of the columns in response to a column address, and a plurality of sense amplifier groups are connected with the selected columns by the column selector circuit. The column selector circuit variably selects the columns according to whether the column address is 4N-aligned (where N is an integer having a value of 1 or more). For example, the column selector circuit chooses columns of the column address when the column address is 4N-aligned, and chooses columns of an upper column address when the column address is not 4N-aligned.